



28147

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Nobutoshi AOKI et al.

Attorney Docket 40301/0578

Title: SEMICONDUCTOR INTEGRATED CIRCUIT INCLUDING  
INSULATED GATE FIELD EFFECT TRANSISTOR AND METHOD  
OF MANUFACTURING THE SAME

Appl. No.: 09/440,928

Filing Date: November 16, 1999

Examiner: S. Rao

Art Unit: 2814

12/9/02  
Line  
(3 mo)  
Mallory  
12-9-02  
RECEIVED  
NOV 21 2002  
TECHNOLOGY CENTER 2800

**PETITION FOR EXTENSION OF TIME**  
**UNDER 37 C.F.R. § 1.136**

Commissioner for Patents  
Washington, D.C. 20231

Sir:

It is respectfully requested that an extension of time for the period indicated below be granted in accordance with the provisions of 37 C.F.R. § 1.136 to take the action required in the application identified in caption, as reflected by the papers submitted herewith.

—	First Month	\$ 110	(\$ 55)*
<u>X</u>	Second Month	\$ 290	(\$145)*
<u>X</u>	Third Month	\$ 520	(\$260)*

**TOTAL FEE: \$810.00** \*(Small Entity)

**(FIRST MONTH EXTENSION PAID ON SEPTEMBER 30, 2002)**

A check in the amount of the above Total Fee is attached. This amount is believed to be correct; however, the Commissioner is hereby authorized to charge any deficiency or credit any overpayment to Deposit Account No. 19-0741. If one or more (additional) extension(s) of time is/are required for the filing of this paper, such extension(s) is/are hereby expressly petitioned for and the Commissioner is authorized to charge the required fee to Deposit Account No. 19-0741.

November 19, 2002  
Date

FOLEY & LARDNER  
3000 K Street, N.W., Suite 500  
Washington, D. C. 20007-5109  
Telephone: (202) 672-5300

Respectfully submitted,

Aaron C. Chatterjee

Richard L. Schwaab  
Reg. No. 25,479

Aaron C. Chatterjee  
Reg. No. 41,398

11/20/2002 SDENB081 00000031 09440928 810.00 DP  
01 FC:1253